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WT8045

Synchronous Signal Discriminator and Power Saving Detector for Green Monitor

May 4, 1995

DESCRIPTION

The WT8045 is a silicon monolithic circuit designed for synchronous signal processing and power saving detection of multi-sync display monitors, which can cope with many kinds of PC's and workstations.

It can be applied to display monitors supporting standard IBM VGA, VESA super VGA and IBM 8514/A video modes. It can also be used in other high-end display monitors supporting non-standard video modes with user-defined horizontal/vertical frequency ranges.

The WT8045 incorporates many functional circuits, including horizontal/vertical frequency discrimination, display mode selection, and synchronous pulse polarity and power saving detection, into this single chip IC.

WT8045 is more convenient for you to shrink the PC board size and to reduce the material and labor cost with fewer components.

FEATURES

- Accepting two separated H&V synchronous signals with positive/ negative polarity.
- Support VESA VGA (640X480, 640X400, 640X350), VESA SVGA (800X600), European SVGA (800X600), VESA new SVGA (800X600), XGA (1024X768) and 1280x1024.
- Capable of processing horizontal frequency between 25KHZ to 80KHZ.
- Standard IBM video mode control outputs (1024X768, 640X480, 640X400, 640X350).
- Five non-standard horizontal frequency control outputs in predefined frequency range.
- Power saving mode - It can detect the conditions of monitor to decide which one will be selected as following: ON/STANDBY/SUSPEND/OFF mode.
- Fixed polarity outputs on both horizontal and vertical synchronous signals.

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- Power supply voltage: DC 5 volts; but for those pins with open-drain structure, such like the mode select control output and frequency discrimination control output pins, can be connected to 12 volts through pull-high resistor.

APPLICATION

- Auto size control for Multi-Sync Display Monitors

ORDERING INFORMATION

Part No.	Package	Note
WT8045N24P1	P-DIP 24L	V * 128
WT8045N24P3	P-DIP 24L	Without Mute
WT8045N24P4	P-DIP 24L	Without Mute
WT8045N24P5	P-DIP 24L	V * 1
WT8045N24P6	P-DIP 24L	With Mute
WT8045N24P7	P-DIP 24L	Without Mute
WT8045N24P8	P-DIP 24L	With Mute
WT8045N28P1	P-DIP 28L (skinny)	V * 128 Without Mute
WT8045N28P2	P-DIP 28L (skinny)	V * 128 Without Mute
WT8045N28P3	P-DIP 28L (skinny)	V * 1 Without Mute
WT8045N28P4	P-DIP 28L (skinny)	V * 128 With Mute
WT8045N28P5	P-DIP 28L (skinny)	V * 1 With Mute
WT8045N28P6	P-DIP 28L (skinny)	V * 1 Without Mute
WT8045N28P7	P-DIP 28L (skinny)	V * 128 With Mute
WT8045N28P8	P-DIP 28L (skinny)	V * 1 With Mute
WT8045N32	P-DIP 32L	--

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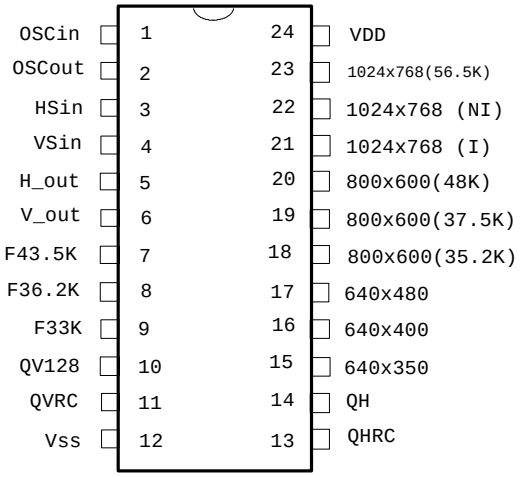
PIN CONFIGURATION

WT8045N24P1



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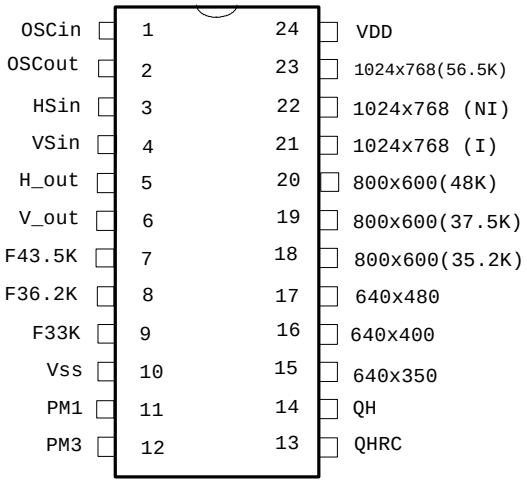

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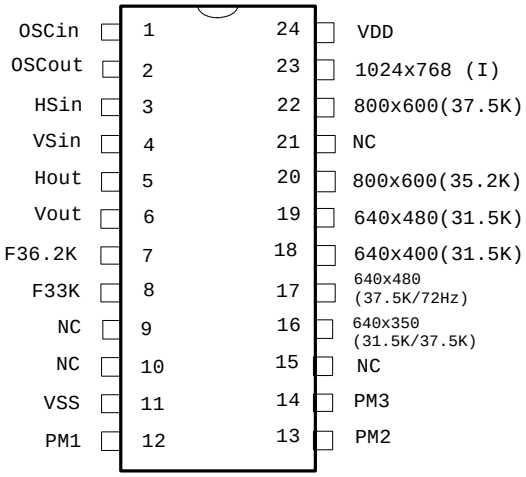

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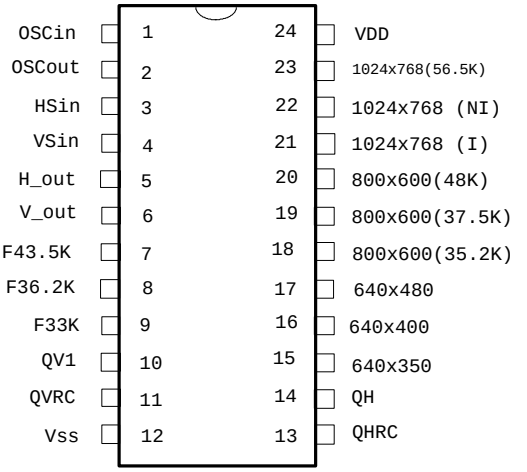

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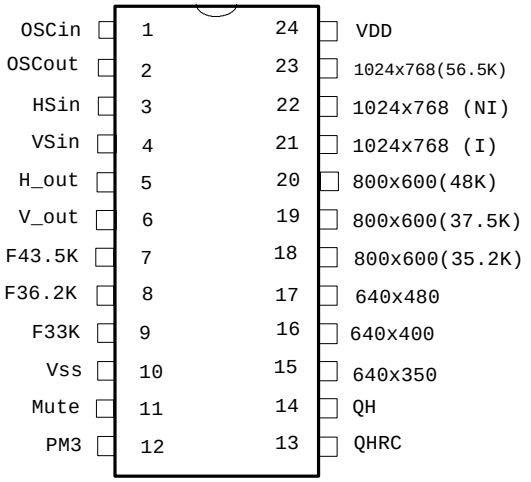
WT8045N24P6



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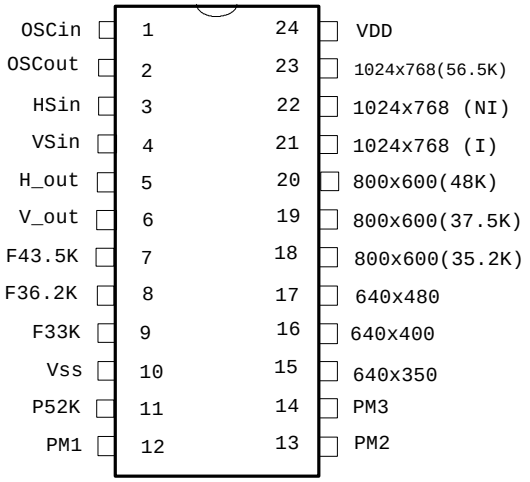

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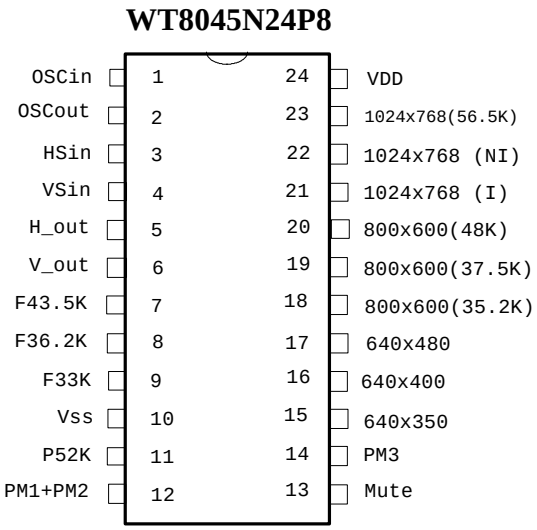
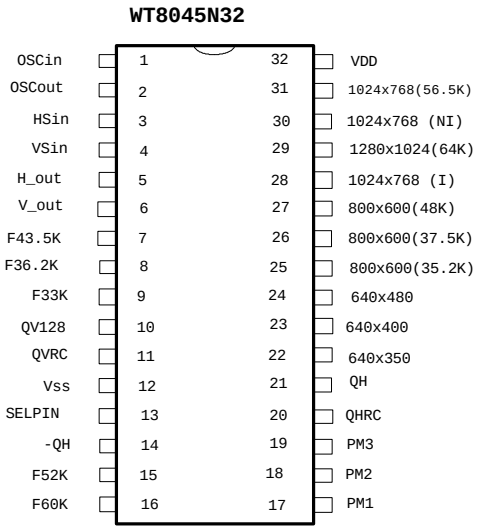


WT8045N32



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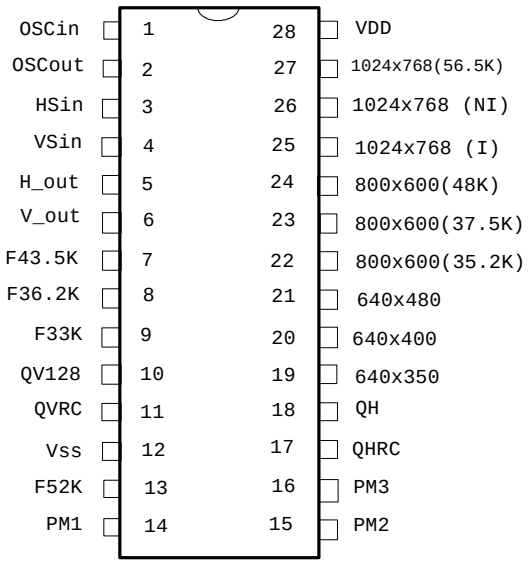
WT8045N28P1



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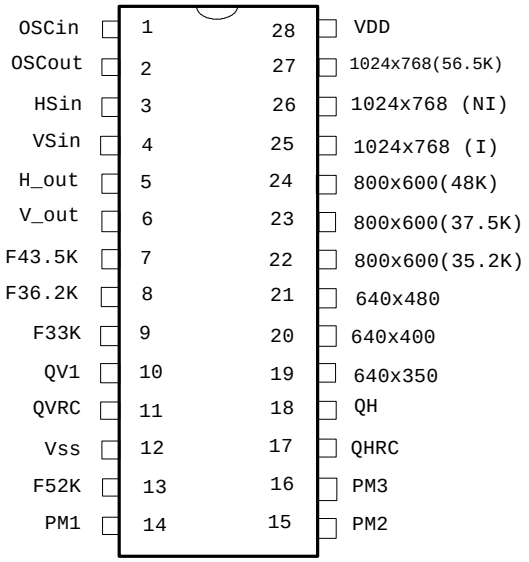

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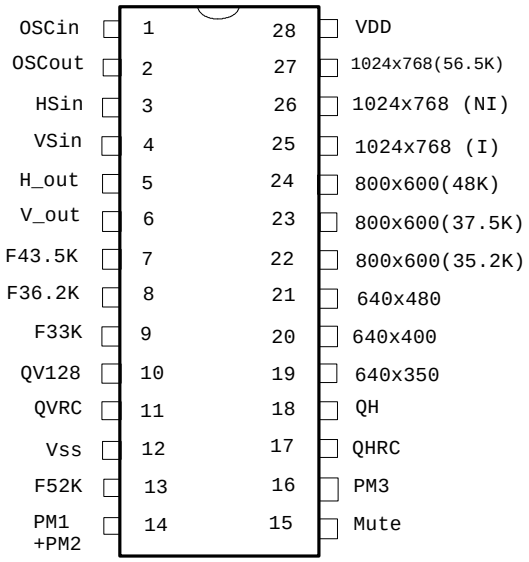
WT8045N28P4



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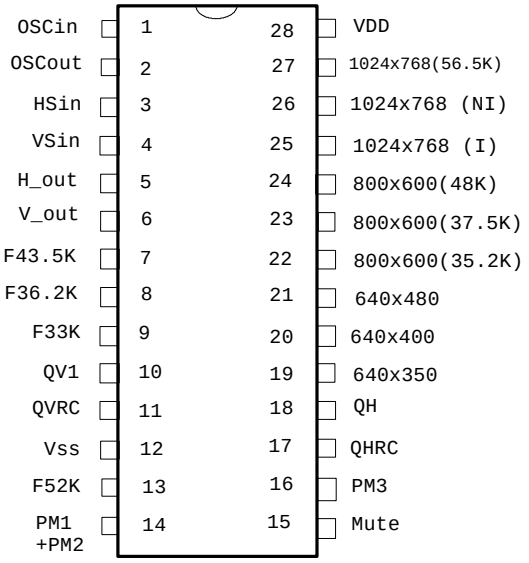

Note: The Hout and Vout pin of N28P1, N28P3, N28P4 and N28P5 are negative pulse.

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ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	VALUE	UNIT
Digital Supply Voltage	V_{DD}	5.5	V
Horizontal Sync. Input Voltage	V_{HS}	V_{DD}(5)+0.3	V_{PP}
Vertical Sync. Input Voltage	V_{VS}	V_{DD}(5)+0.3	V_{PP}
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{OPT}	0¡ ã70	¢ J
Storage Temperature Range	T_{STG}	-40¡ ã125	¢ J

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Digital Supply Voltage	V_{DD}(5)	4.5	5	5.5	V
Supply Current (Standby)	I_P			13	mA
Synchronous Input Voltage Low	V_{IL}			0.8	V_{PP}
Synchronous Input Voltage High	V_{IH}	2.4	4	5.5	V_{PP}
Horizontal Synchronous Frequency Range	F_H	25	¡ Ð	80 (for N32)	KHz
Vertical Synchronous Frequency Range	F_V	50	¡ Ð	120	Hz
Crystal Clock Frequency	F_{CLK}	3.5764	3.58	3.5836	MHz
Open Drain Pull High Voltage	V_{OH}			12	V
Resistance of Monostable for Hsin	R_H	10		100	K£ [
Capacitance of Monostable for Hsin	C_H	¡ Ð	100	¡ Ð	pF
Resistance of Monostable for Vsin	R_V	10		500	K£ [
Capacitance of Monostable for Vsin	C_V	¡ Ð	100	¡ Ð	pF

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ELECTRICAL CHARACTERISTICS

(V_{DD}=5V, T_{OPT}=25°C, Crystal=3.58MHz)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Discrimination of H. Synchronous Frequency	F33K	32.9	¡ Ð	33.1	KHz
	F36.2K	36.1	¡ Ð	36.3	KHz
	F43.5K	43.4		43.6	KHz
	F52K	51.9	¡ Ð	52.1	KHz
	F60K	59.9	¡ Ð	60.1	KHz
Output Low (H-out, V-out), when I_{OL} = 4mA	V_{OL1}			0.4	V_{PP}
Output High (H-out, V-out), when I_{OH} = -400£ gA	V_{OH1}	2.4			V_{PP}
Open Drain Output Low when I_{OL} = 6mA	V_{OL2}			0.4	V_{PP}
Output Sink Current (H-out, V-out) when V_{OL1} = 0.4V	I_{OL1}			4	mA
Output Drive Current (H-out, V-out) when V_{OH1} = 2.4V	¡ W$_{OH1}$¡ W			400	£ gA
Open Drain Sink Current when V_{OL2} = 0.4V	I_{OL2}		10		mA
Open Drain Sink Current when V_{OL2} = 5V	I_{OL2}		40		mA

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MONO_STABLE DYNAMIC ELECTRICAL CHARACTERISTICS

(Ta=25°C; Input t_r,t_f=20ns, C_L=50PF)

ITEM	MIN.	TYP.	MAX.	UNITS
Input H_SYNC Pulse Width	0.558	¡ Ð	4	£ §
Input V_SYNC Pulse Width	0.0384	¡ Ð	0.125	ms
Output Pulse Transition Time	¡ Ð	100	200	ns
Output Pulse Propagation Delay	¡ Ð	300	600	ns
Output Pulse Width Adjust Range	10	¡ Ð	90	¢ M
H_MONO_STB:				
31KHz¡ Ð37.5KHz			26.66	£ §
31KHz¡ Ð48KHz			20.83	£ §
31KHz¡ Ð57KHz			17.54	£ §
31KHz¡ Ð64KHz			15.62	£ §
V_MONO_STB:				
(50Hz¡ Ð120Hz)*128				
6.4KHz¡ Ð5.36KHz			65.10	£ §
(50Hz¡ Ð80Hz)*128				
6.4KHz¡ Ð0.2KHz			97.66	£ §
(50Hz¡ Ð120Hz)*1		10		ms
Typical Pulse width Variation as a function of Temperature at 75¢ Jto 24 ¢ J	¡ Ð	¡ Ð	¡ Ó	¢ M
Typical Pulse Width Variation as a function of Supply Voltage at 4.75V to 5.25V	¡ Ð	¡ Ð	¡ Ó	¢ M
Output Low (Sink) Current	1	¡ Ð	6	mA
Output Voltage Low-Level	¡ Ð	0	0.05	V
Output Voltage High-Level	4.95		¡ Ð	V
Output Jitter (Hout & Vout) Hin & Vin Rise time and Fall time = 200ns			5	ns

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APPLICATION INFORMATION

Name	Function	Struncure of Terminal
OSCin	A clock generating circuit is built into the chip. So if a resonator is connected to OSCin/OSCout, a clock signal can be obtained	I
OSCout	Refer to OSCin pin	O
Hsin	Input terminal of horizontal synchronous signal	I, TTL compatible
Vsin	Input terminal of vertical synchronous signal	I, TTL compatible
H_OUT	Output pin, fixed negative polarity of original H_SYNC signal with same pulse width (but, positive for N28P2, N28P6,N28P7 and N28P8)	I, TTL compatible
V_OUT	Output pin, fixed negative polarity of original V_SYNC signal with same pulse width (but, positive for N28P2, N28P6,N28P7 and N28P8)	O, TTL compatible
F43.5k	>43.5k then active low, <43.5k then high	O, open drain
F36.2k	>36.2k then active low, <36.2k then high	O, open drain
F33k	>33k then active low, <33k then high	O, open drain
QV	Output pin, fixed positive polarity of vertical signal; pulse width depend upon RV & CV.	O, open drain
QVRC	Input pin, connected to Vdd through RV & to ground through CV	I
Vss	Ground	
SELPIN	Input pin, to select which one of H_SYNC or V_SYNC appears on the output pin of QV; N.C. selects the V-SYNC on the output, grounding selects the H_SYNC.	I, (N.C.-no connection)
-QH	Output pin, fixed negative polarity of horizontal signal; pulse width depend upon RH & CH.	O, open drain
F52k	>52k then active low, <52k then high	O, open drain
F60k	>60k then active low, < 60k then high	O, open drain
PM1	Indicate in STAND-BY mode	O, open drain

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Name	Function	Struncure of Terminal
PM2	Indicate in SUSPEND mode	O, open drain
PM3	Indicate in OFF mode	O, open drain
QHRC	Input pin, connected to Vdd through RH & to ground through CH.	I
QH	Output pin, fixed positive polarity of horizontal signal; pulse width depend upon RH & CH	O, open drain
640¡ Ñ50	Mode select control output, if IBM VGA 640¡ Ñ50 mode, or VESA VGA 640¡ Ñ50 mode. Then active "low", else open state output	O, open drain
640¡ Ñ80	VESA VGA mode 640¡ Ñ80 (37.5k/72Hz)	O, open drain
640¡ Ñ00	If IBM VGA 640¡ Ñ00 mode, or VESA VGA 640¡ Ñ00 mode then active "low" (640¡ Ñ00, 31.5k, for N24P4)	O, open drain
640¡ Ñ80	If IBM VGA 640¡ Ñ80 mode, or VESA VGA 640¡ Ñ80 mode then active "low" (640¡ Ñ80, 31.5k, for N24P4)	O, open drain
800¡ Ñ00	VESA super VGA mode (H_SYNC = 35.2k, V_SYNC = 56Hz)	O, open drain
800¡ Ñ00	European super VGA mode (H_SYNC = 37.5k, V_SYNC = 60Hz)	O, open drain
800¡ Ñ00	VESA new super VGA mode (H_SYNC = 48k, V_SYNC = 72Hz)	O, open drain
1024¡ Ñ 768(I)	IBM 8512/A interlace mode (H_SYNC = 35.5k, V_SYNC = 86Hz)	O, open drain
1280¡ Ñ 1024	1280¡ Ñ1024 mode control output (H_SYNC = 64k, V_SYNC = 60Hz)	O, open drain
1024¡ Ñ 768(NI)	IBM 8514/A non-interlace mode (H_SYNC = 48.5k, V_SYNC = 60Hz)	O, open drain
1024¡ Ñ 768(57k)	XGA 1024¡ Ñ768 mode Hsync freq. 57kHz (H_SYNC = 56.5k, V_SYNC = 72Hz)	O, open drain
Vdd	5 Volts power supply	

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APPLICATION DESCRIPTION

DPMS (Display Power Management Signaling) Detection

As per DPMS proposal version 1.0P, revision 0.54P, WT8045 provides Monitor Power Management Detection Circuit for the convenience of monitor designers in designing power saving monitors, or the so called "Green Monitors". Please refer to the table 1 as below for power states defined in the DPMS.

DPMS requires at least 5 seconds delay before transition from ON state to any power saving state, to avoid unintentionally entering a power saving state during display resolution changes and timing mode changes. And it can be done instantaneously, for the transition between any power saving state.

Table 1 Display Power Management Summary

State	Signals			DPMS Compliance Requirement	Power Savings	Recovery Time
	Horizontal	Vertical	Video			
On	Pulses	Pulses	Active	Mandatory	None	Not Applicable
Stand-by	No Pulses	Pulses	Blanked	Optional	Minimal	Short
Suspend	Pulses	No Pulses	Blanked	Mandatory	Substantial	Longer
Off	No Pulses	No Pulses	Blanked	Mandatory	Maximum	System Dependent

* "No-Pulse" represents the frequency of Hsin or Vsin less than or equal to 10Hz, but "Pulses" represents that frequency of Hsin greater than or equal to 10KHz and Vsin greater than or equal to 40Hz

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The way WT8045 implements VESA DPMS

As shown on Table 2, WT8045 use PM1 to represent Stand-by State, PM2 as Suspend State and PM3 as OFF State. When H_SYNC / V_SYNC signals transition from ON State to any one of the three power saving states, WT8045 will delay 5.9 seconds to meet the VESA DPMS requirement: the minimum 5 seconds delay to avoid unintentionally entering a power saving state during display resolution and timing mode changes. If during this delay time period, H_SYN and V_SYN signals return to ON State, then all three power management pins (PM1, PM2 and PM3) will remain ON state. If power management state of H_SYNC and V_SYNC prolong for more than 5.9 seconds, then these three power management pins will change to the corresponding states. While changing from any power saving state back to ON State will take about 0.368 second for H_SYNC / VSYNC pulse checking. And transition between any power saving state will be done immediately.

Table 2: The truth table of Power Saving Detector

MODE	Hsin	Vsin	PM1	PM2	PM3
ON	Pulses	Pulses	1	1	1
STAND_BY	No Pulses	Pulses	0	1	1
SUSPEND	Pulses	No Pulses	0	0	1
OFF	No Pulses	No Pulses	0	0	0
OVERRIDE	No Pulses	No Pulses	1	1	1
	Manually PWR ON				

OVERRIDE mode:

To initial override, both horizontal and vertical sync signals shall be in the no pulses condition when the display is maintained during the entire time override is required. As soon as pulses are detected on horizontal and vertical sync signal. The display shall enter DPMS operation.

Three power management pins are open drain structure and active low. If you do not need all those three power saving states in your design. You can just short two or three pins of the pins PM1/PM2/PM3. for example, by shorting pin PM1 and pin PM2, you will have only two power saving states, that is OFF and Suspend states, so you have three states total, including ON State. Please refer to Application Circuit 2.

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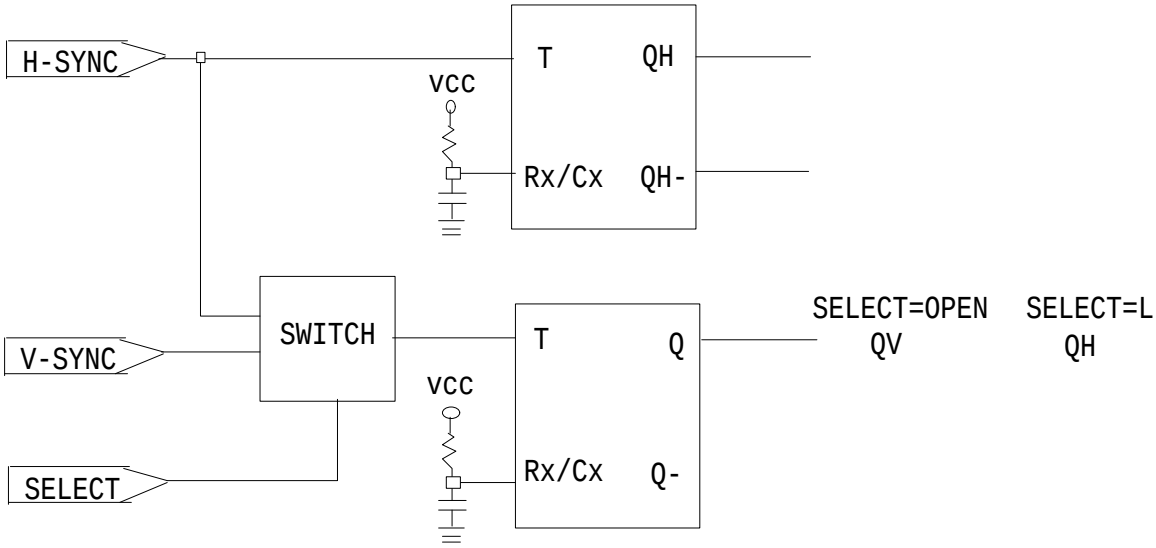
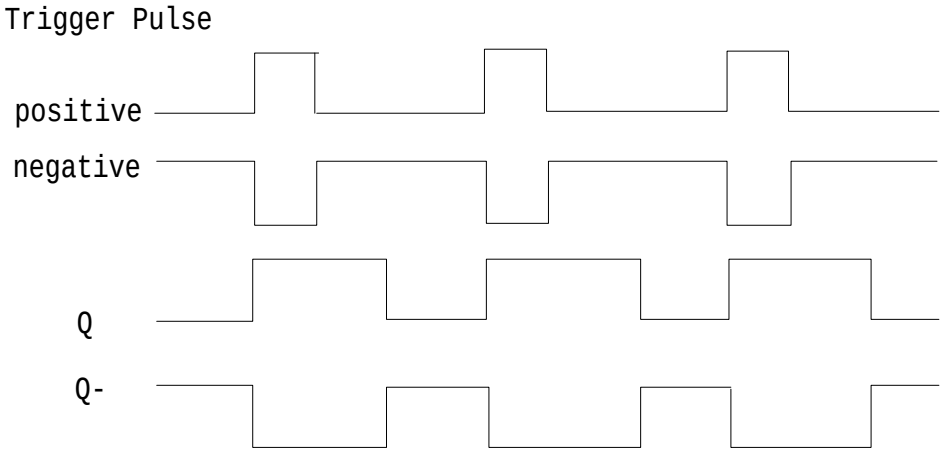
Mono_Stable Circuit

WT8045 includes two sets of Mono_Stable Circuits, one uses H_SYNC as trigger signal, the other uses either H_SYNC or V_SYNC as trigger signal (this only can be done on 32 pin package, for 24 pin and 28 pin packages the trigger signal is fixed to H_SYNC); for N24p4 package, there is no mono-stable circuit. Please refer to the figure as below:



The Mono_Stable Circuit is triggered by positive edge, no matter H_SYNC or V_SYNC is used as trigger signal. Please refer to the timing chart as below:



The output of Mono_Stable Circuit is open drain structure, and can be pulled up to +12V maximum.

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In case of using output pulse of V_MONO_STABLE as voltage source, in order to prevent the problem of slow response time, causing from the low frequency on vertical synchronous signal, WT8045 internally increases the vertical signal frequency to 128 times the original frequency, that is from 50Hz - 120 Hz to 6.4KHz - 15.36KHz. Then WT8045 uses this increased frequency as the input signal of MONO_STABLE, so the leading edge of the signal of the increased frequency will trigger the MONO_STABLE circuit.

An external resistor (Rx) and an external capacitor (Cx) control the timing and accuracy of the circuit. Adjustment of Rx and Cx provides a wide range of output pulse widths from the Q and Q-bar terminals. The delay time from trigger input to output transition is independent of Rx and Cx.

The minimum value of external resistor Rx is 10k ohms. The typical value of external capacitor Cx is 100 pF. The time period (T) for this multi-vibrator can be calculated with the formula: $T \approx 1.1\ Rx \bullet Cx$.

H/V Frequency Divisions and Video Modes

Figure 1 illustrates the typical frequency ranges of H and V sync signals for display monitors. The operating video modes are determined by the H and V frequencies, and occasionally, by their polarities. The typical video modes of display monitors include the IBM VGA, VESA VGA, European VGA/super VGA, VESA super VGA, IBM 8514/A, XGA, and 1280x 1024.

WT8045 can determine 13 standard video modes for 32 pin package (refer to Table 3) according to H and V frequencies and polarities. These standard video modes include the IBM VGA, VESA VGA, VESA super VGA and IBM 8514/A. This provides the users with the capability to adjust the screen size for different modes.

WT8045 pre-sets the discriminating points both on H and V frequencies. The discriminating points for H sync are 33KHz, 36.2KHz, 43.5KHz, 52KHz and 60KHz (for 32 pin). These discriminating points will be able to identify various video modes as shown in Fig. 1. WT8045 also provides the flexibility for users to define these discriminating points through mask option.

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The tolerance for H sync frequency discrimination is¡ Ó.1KHz. For instance, the 33KHz discriminating point will be able to distinguish the H sync frequency that is either "less than or equal to" 32.9KHz, or "greater than or equal to" 33.1KHz. There is an ambiguous region between 32.9KHz and 33.1KHz.

WT8045 has two discriminating points, 64Hz and 78Hz, for the V sync signal as shown in Fig.1. The tolerance is ¡ Ó.4Hz. The discrimination results of V sync frequency are used internally for mode selection.

Base on the package consideration, IBM VGA mode and VESA VGA mode (both have same resolution: 640x480, 640x400, 640x350) are decoded on same open Drain structure output pins. In case of these whole six modes decoding is needed, the horizontal frequency discrimination pin F33k or F36.2k must take into consideration. The horizontal frequency of IBM VGA mode is 31.5kHz, and VESA IBM VGA mode is 37.5kHz. Using F33k or F36.2k pin can clearly identify these two standard modes. The decoding circuit is attached on application section for reference.

Graphic Standard	Resolution	Horizontal	Vertical	Polarities
IBM VGA	640X350	31.5kHz	70Hz	+,-
	640X400	31.5kHz	70Hz	-,+
	640X480	31.5kHz	60Hz	-.-
VESA Super VGA	800X600	35.2kHz	56Hz	
IBM 8512/A Interlaced	1024X768	35.5kHz	86Hz	
VESA VGA	640X350	37.5kHz	83Hz	+,-
	640X400	37.5kHz	83Hz	-,+
	640X480	37.5kHz	72Hz	-,-
European Super VGA	800X600	37.5kHz	60Hz	
VESA New Super VGA	800X600	48.0kHz	72Hz	
IBM 8514/A Non-Interlaced	1024X768	48.5kHz	60Hz	
VESA New 1024X768	1024X768	56.5kHz	72Hz	
Work Station 1280X1024	1280X1024	64.0kHz	60Hz	

Table 3: Graphic Standard and Frequencies

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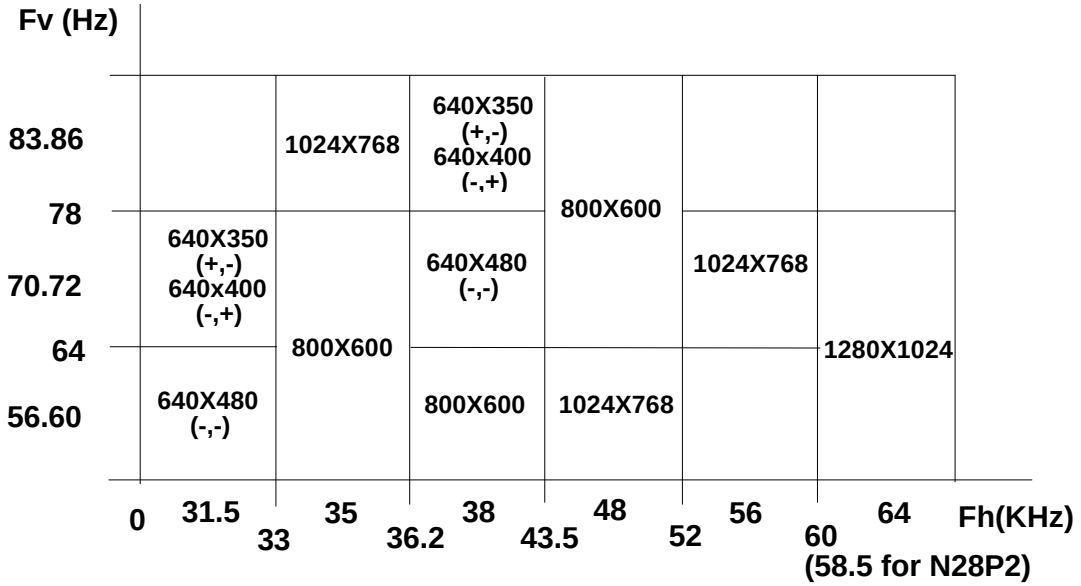

Figure 1: H/V Frequency Division and Video Mode

Mode	PIN	640X480	640X400	640X350
IBM	640X480	0	1	1
	640X400	1	0	1
VGA	640X350	1	1	0
VESA	640X480	0	1	1
	640X400	1	0	1
VGA	640X350	1	1	0

Table 4: IBM VGA/ VESA VGA Decoding Table

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Horizontal Frequency Discriminator

There are horizontal frequency discriminator pins on different type package: 33k, 36.2k (for N24P4 package); 33k, 36.2k, 43.5k (for 24 pin); 33k, 36.2k, 43.5k, 52k (for 28 pin); 33k, 36.2k, 43.5k, 52k, 60k (for 32 pin); please refer to table 5 for the logical truth table of these pins. These frequency discriminator pins output can be used for C_S Capacitor Control directly as well as other application.

Signal Hsync	F33k	F36k	F43.5k	F52k	F60k
Hs<33k	1	1	1	1	1
36k>Hs>33k	0	1	1	1	1
43.5k>Hs>36k	0	0	1	1	1
52k>Hs>43.5k	0	0	0	1	1
60k>Hs>52k	0	0	0	0	1

Table 5: Truth table of Frequency discriminator

Mute function Timing Diagram

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APPLICATION CIRCUIT I

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APPLICATION CIRCUITII

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APPLICATION CIRCUIT III

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APPLICATION CIRCUIT IV

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DIP OUTLINE DIMENSIONS

	A	B	C	D	E	F	G
N24	1250	542	152	100	130	650	600
N28 SKINNY	1385	288	130	100	130	355	310
N32	1650	542	154	100	130	650	600

¡ ¯Dimension in mil
¡ ¯1mm = 39.37 mil

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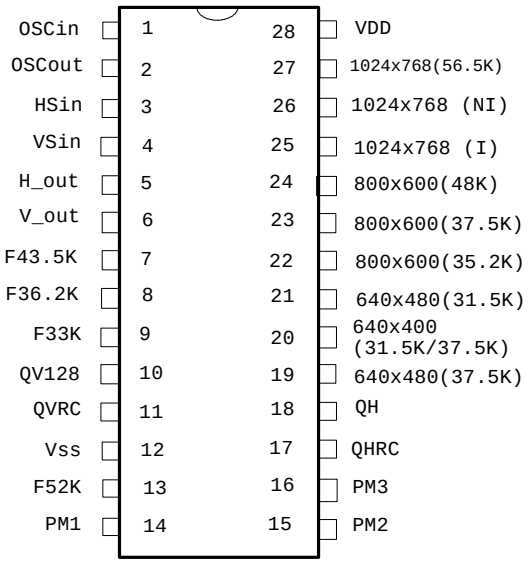
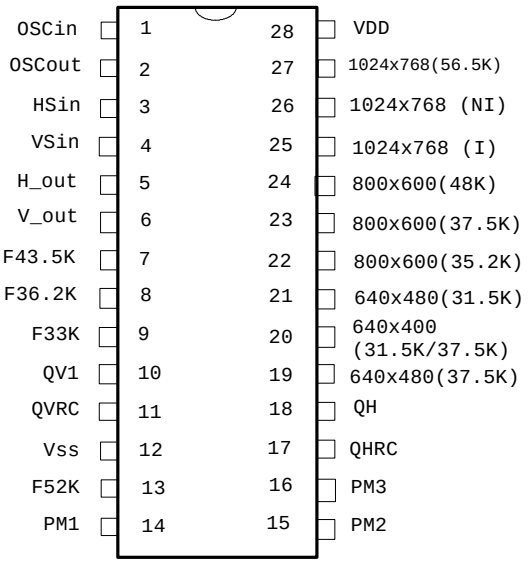
WT8045N28P2



WT8045N28P6



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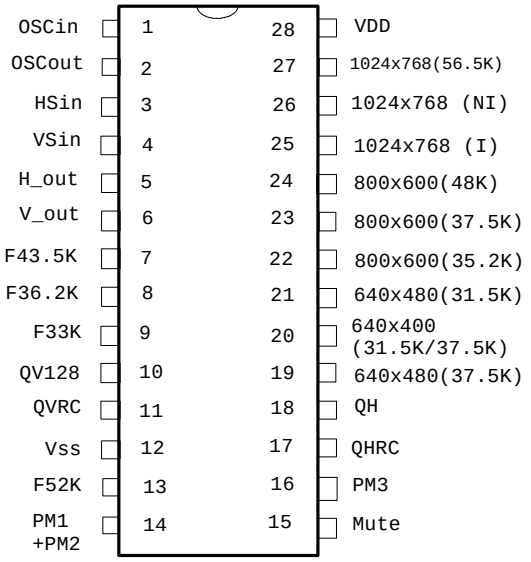

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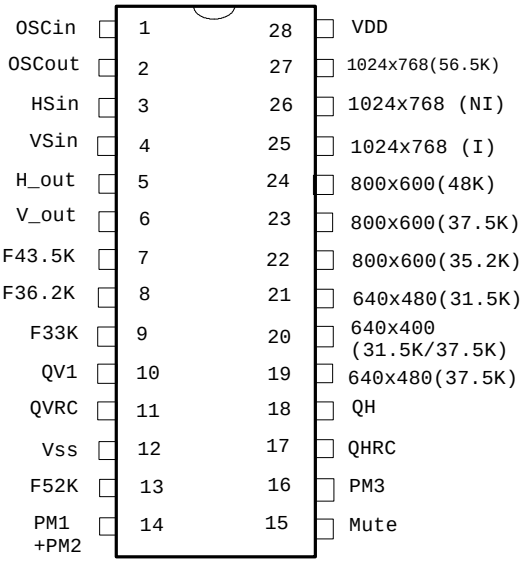

Note: The Hout and Vout pin of N28P2, N28P6, N28P7 and N28P8 are positive pulse.

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